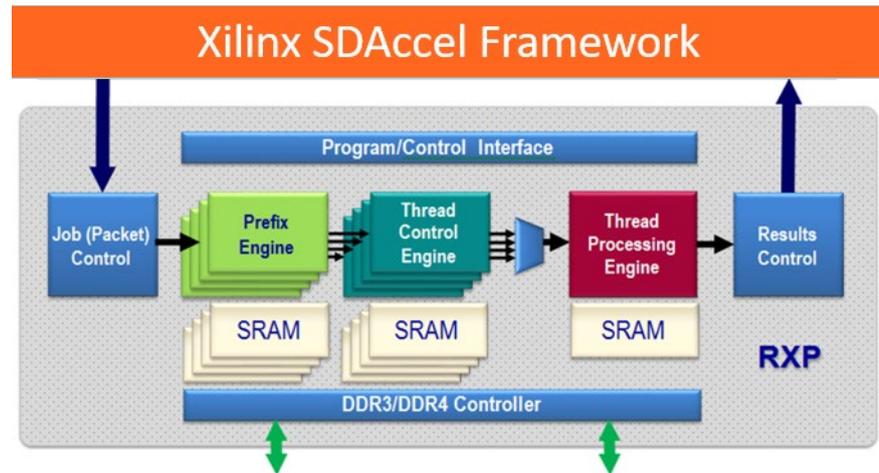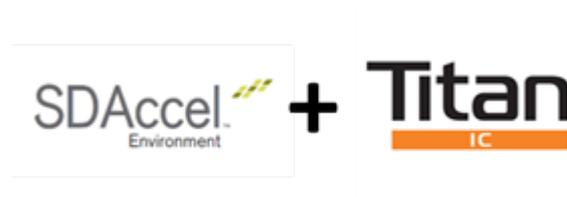# SDACCEL

RXP ON XILINX SDACCEL™ PLATFORM

ACCELERATED DATA CENTER APPLICATIONS

The latest Xilinx SDAccel platform, embedded with Titan IC's Regular Expression Processor RXP, offers a fully-flexible and efficient solution for developers to build and maintain high performance networks able to manage larger workloads while not overloading the CPU cores. SDAccel offers a dynamic, easy-to-use card to configure acceleration in data center applications using standard programming languages.

PRODUCT OVERVIEW

Software engineers can use the SDAccel building blocks to build a high throughput network with a high rule density that requires Regular Expression pattern matching. When compared to software solutions, RXP generates a 10X+ improvement in throughput and can support up to 1 million rules to achieve significant CPU offload and free up network resources. This considerable boost in acceleration combined with the flexibility of the SDAccel framework makes this a highly-dynamic tool for data center developers.

Additional IP blocks can be added at any stage to produce a fully-flexible, modifiable platform on which developers can build the inspection components that will grow with the needs of the network.

SOFTWARE APPROACH TO HARDWARE ACCELERATION

Titan IC's RXP Processor within the Xilinx SDAccel platform work together to provide customers with a software defined hardware acceleration solution for high-throughput, low-latency applications that require Regular Expression pattern matching for network analysis and log file analytics.

KEY FEATURES..

❖ Enhanced security analytics acceleration
❖ Flexible platform for high throughput/high rule density networks
❖ Easy to build & configure modular security/data analytics products on FPGA
❖ Compatible with Xilinx® Alveo™ Data Center accelerator cards
❖ Enables CPU offload and increased host processor capacity

KEY BENEFITS..

❖ Easy to use off-the-shelf solution
❖ Dynamic configurability
❖ Optimum acceleration up to 100Gb/s
❖ Significant CPU offload
❖ Scans up to 1 million regular expression rules
❖ Reduces engineering design effort
❖ Lower costs
❖ Faster time-to-market

CONCLUSION

This dynamically configurable solution provides a future proof hardware platform on FPGA that allows customers to tailor their configurations to their exact needs.

Combining SDAccel with the RXP processor within the same framework is one of the first ever instances of a third-party SDAccel release core which provides customers with an easily-configurable solution to meet their varying inspection workloads and to optimize acceleration on the network.