HELIOS RXP FOR FPGA

SOFT IP FOR FPGA SECURITY ANALYTICS ACCELERATION

Offload and accelerate the analysis of networks and detection of threats

Perform many thousands of complex, parallel searches at line speed

Designed for SmartNIC FPGA & Solid State FPGA Applications

Helios RXP for FPGA is a unique, fully scalable, hardware accelerated solution for security analytics acceleration and content processing.

It is designed to deliver high throughput, low latency content analytics, Deep Packet Inspection (DPI) and pattern/string matching using Regular Expressions (RegEx). It can be tuned for the desired combination of throughput, rule depth and complexity.

HIGHLIGHTS

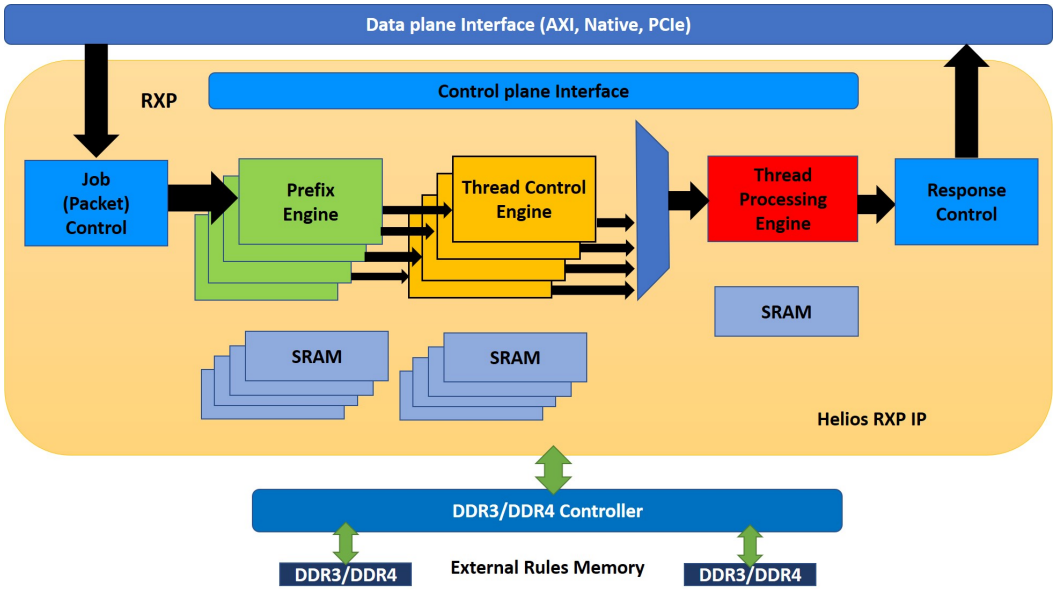
- **Accelerated Throughput** - perform complex data searches at speeds up to 40Gb/s
- **In-depth Packet Inspection** - complex and comprehensive pattern matching
- **High Capacity Content Analysis** - Supports up to 1M RegEx rules using external DDR3/4
- **High Scalability** – scalable bandwidth from 5Gb/s to 100Gb/s
- **CPU Offload** - Offload of data analytic functions from host CPU freeing up CPU cores and saving costs
- **High Throughput Performance per Watt –** reduced heat dissipation and operating costs
- **Easy Compatibility** - supports POSIX/PCRE compatible regular expressions to detect malware, enforce blacklists and run Snort or customer-defined RegEx datasets
- **Engineering Efficiency** - supplied as an FPGA IP block, reducing engineering effort, costs and time-to-market

APPLICATIONS

- Security Analytics Acceleration
- Next Generation Firewall (NGFW)
- Intrusion Prevention System (IPS)
- Distributed Denial of Service (DDoS) Mitigation
- Data Loss Prevention (DLP)
- SmartNIC
- Network Monitoring
- Advanced auditing of user/application security policies
- Rule based content processing for spam, URLs and adware
- Financial data mining – parsing of streamed financial feeds
- Log File Analytics

Titan IC, Concourse One, N.I. Science Park, Belfast, Northern Ireland, BT3 9DT
+44 (0)28 9045 3512 info@titan-ic.com @TitanICSystems

BLOCK DIAGRAM



CAPABILITIES & RESOURCES

The comprehensive SDK includes:

- RXP Compiler
- Application Programming Interface (API) for plugin development
- Reference applications
- Utilities

Helios RXP technology is optimised for Xilinx FPGA, Kintex® UltraScale™, Virtex® UltraScale™ and Virtex® UltraScale+ platforms, and can be configured for bandwidths ranging from 5 to 100Gb/s. Resource requirements for running at a core clock rate of 160MHz are shown below:

	Helios RXP for FPGA Resource Requirements Xilinx KU115, Helios V5.8		Helios RXP for FPGA Resource Requirements Xilinx VU9P, Helios V5.8	
Bandwidth	20Gb/s	40Gb/s	50Gb/s	100Gb/s
Rules Capacity (up to)	1 million	1 million	1 million	2 million
# BRAMs	904	1655	573	1290
#URAM	N/A	N/A	308	620
# LUTs	113K	216K	424K	658K
# FFs	130K	241K	424K	758K

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